

Documents

Hussain, A.A., Tayem, N., Soliman, A.-H., Radaydeh, R.M.

FPGA-Based Hardware Implementation of Computationally Efficient Multi-Source DOA Estimation Algorithms

(2019) *IEEE Access*, 7, art. no. 8753477, pp. 88845-88858.

Abstract

Hardware implementation of the proposed direction of arrival (DOA) estimation algorithms based on Cholesky and LDL decomposition is presented in this paper. The proposed algorithms are implemented for execution on a field programmable gate array (FPGA) as well as a PC (running LabVIEW) for the multiple non-coherent sources located in the far-field region of a uniform linear array (ULA). Prototype testbeds built using the national instruments (NI) universal software radio peripheral (USRP) software defined radio (SDR) platform and Xilinx Virtex-5 FPGA are originally constructed for the experimental validation of the proposed algorithms. The results from LabVIEW simulations and real-Time hardware experiments demonstrate the effectiveness of the proposed algorithms. Specifically, the implementation of the proposed algorithms on a Xilinx Virtex-5 FPGA using the LabVIEW software clarifies their efficiency in terms of computation time and resource utilization, which make them suitable for the real-Time practical applications. Moreover, the performance comparison with the QR decomposition-based DOA algorithms as well as similar FPGA-based implementations reported in the literature is conducted in terms of the estimation accuracy, computation speed, and FPGA resources consumed. © 2013 IEEE.

2-s2.0-85069754879

Document Type: Article

Publication Stage: Final

Source: Scopus

Access Type: Open Access